compares q1(t) and q2(t) to programmable thresholds Q1(1) - Q1(n) and Q2(1) - Q2(n) contained therein.

When q1(t) or q2(t) increases beyond any of the programmable thresholds Q1(1)-Q1(n), or Q2(1)-Q2(n), respectively, then at that time formatter 268 generates and sends the high or low priority variable-rate control code, respectively, to switching fabric 202, instructing it to slow the rate at which it transmits high or low priority data for storage in buffer 260 or 262, respectively. Conversely, when q1(t) or q2(t) decreases below any of the programmable thresholds Q1(1)-Q1(n), or Q2(1)-Q2(n), respectively, then at that time formatter 268 generates and sends the high or low priority variable-rate control code, respectively, to switching fabric 202, instructing it to increase the rate at which it transmits high or low priority data for storage in buffer 260 or 262, respectively. Obviously, it is possible that q1(t) and q2(t) may simultaneously increase beyond or decrease below programmable thresholds Q1(1)-Q1(n), or Q2(1)-Q2(n), respectively. In this situation, formatter 268 may simultaneously generate high and low priority variable-rate control codes. Line card 204 is coupled to switching fabric 202 by a single uplink 230. As a result, only one of the high and low priority variable-rate control codes may be transmitted to switching fabric 202 during a transmission cycle on uplink 230. In this situation, the formatter may send the high and low priority variable-rate control codes in consecutive transmit cycles on uplink 230. Alternatively, where q1(t) and q2(t) simultaneously increase beyond or decrease below programmable thresholds Q1(1)-Q1(n), or Q2(1)-Q2(n), respectively, formatter 268 may generate a control word which contains a first and second variable-rate control codes, where the first control variable-rate code instructs fabric 202 to increase or decrease the rate at rate at which it transmits high data for storage in buffer 260, and where the second control variable-rate code instructs fabric 202 to increase or decrease the rate at rate at which it transmits low data for storage in buffer 262. This control word may be sent to the fabric in a single cycle thereby eliminating the need to send separate control codes in succeeding cycles.

FIG. 3 illustrates one embodiment of formatter 252 shown in FIG. 2b. It is noted that formatter 252 may include additional circuitry for performing other functions. Formatter 252 is shown to include a clocked register 280, compare circuit 282, compare circuits 290(1) through 290(n), memory devices 300(1) through 300(n), and control code generator 312.

Operational aspects of one embodiment of the formatter 252 will be described with reference to the flow chart shown in FIG. 4. At step 316, q(t), the quantity of data stored in buffer 250 at time t, is provided to clocked register 280, compare circuit 282, and compare circuits 290(1) through 290(n). At the same time, q(t-1), the quantity of data stored in buffer 250 in the previous clock cycle t-1, is provided by clocked register 280 to compare circuit 282. At step 318, compare circuit 282 compares q(t) to q(t-1). If q(t) is equal to q(t-1), then the process ends with step 320 where q(t) is clocked into clocked register 280. However, if q(t) does not equal q(t-1), then, compare circuit generates a signal, which is provided to compare circuits 290(1) through 290(n), indicating that q(t) is either greater than or less than q(t-1). The process proceeds to step 322, where compare circuits 290(1) through 290 (n) compare q(t) to thresholds Q(1) through Q(n), respectively, stored in memories 290(1) through 290(n), respectively. If q(t) does not equal any of the thresholds Q(1) through Q(n), then the process ends with step 320. However, if q(t) equals one of the thresholds Q(1) through Q(n), then one of the compare circuits 290(1) through 290(n) generates either a rate change signal indicating that the data transmit rate between line card 204 and switching fabric 202 should be increased or decreased depending on whether the signal provided by compare circuit 282 indicates q(t) is greater than q(t-1) or less than q(t-1), respectively. More particularly, when one of the compare circuits 290(1) through 290(n) detects equality between q(t) and one of the thresholds Q(1) through Q(n), the one of the compare circuits 290(1) through 290(n) generates the rate change signal indicating that the data transmit rate between line card 204 and switching fabric 202 should be increased if q(t) is greater than q(t-1) as shown in step 324 or decreased if q(t) is less than q(t-1) as shown in step 326, respectively.

Control code generator 312 receives the rate change signal from one of the compare circuits 290(1) through 290(n). Although not shown within the figures, control code generator 312 may include a programmable memory storing data transmit rate values R(1) through R(n) corresponding to the threshold values Q(1) through Q(n), respectively. Data transmit rate values R(1) through R(n) define differing rates for transmitting data between switching fabric 202 and line card 204. Data transmit rate values R(1) through R(n) vary between R(1) which may equal the fullest possible rate at which data can be transmitted between switching fabric 202 and line card 204, to R(n) which may equal zero transmission rate. Moreover, control code generator 312

is configured to "remember" the current transmit rate, i.e., the rate at which data is being transmitted between switching fabric 202 and line card 204 at time t. In one embodiment, control code generator 312 remembers the current transmit rate using a pointer pointing to one of the data transmit rate values R(1) through R(n). In this embodiment, the data transmit rate value currently being pointed to by the pointer at time t is defined as the current data transmit rate.

FIG. 5 illustrates, in block diagram form, an exemplary programmable memory 350 storing data transmit rate values R(1) through R(n) with a pointer 352 pointing to current data transmit rate R(4). With continuing reference to FIGs. 3 and 4, when control code generator 312 receives a rate change signal from one of the compare circuits 290(1) through 290(n), control code generator, in one embodiment, control code generator moves the position of pointer 352 up one or down one position depending on whether signal from one of the compare circuits 290(1) through 290(n) indicates that the data transmit rate should be increased or decreased, respectively. For example, if the rate change signal from one of the compare circuits 290(1) through 290(n) indicates that the data transmit rate should be increased, then control code generator 312 moves the pointer 352 down to R(3) in FIG. 5. If, on the other hand, the rate change signal from one of the compare circuits 290(1) through 290(n) indicates that the data transmit rate should be decreased, then control code generator 312 moves the pointer 352 up to R(5) in FIG. 5. Further, in response to receiving the rate change signal , control code generator 312 generates and sends a variable-rate control code to switching fabric 202 as shown in step 328 or 330 of FIG. 4. This variable-rate control code includes the data transmit rate value (e.g., R(3) or R(5)) newly pointed to by pointer 352. Switching fabric 202 receives the variable-rate control code and adjusts the data transmission rate between it and the line card 204 in accordance with the data transmit rate value contained in the received variable-rate control code.

In an alternative embodiment not shown in the figures, line card 204 may include a formatter F, a data buffer B that receives data from the fabric 202, a first set of quantity comparators QC(1) through QC(n), a clocked register CR for storing a rate code r(t-1), and a rate comparator RC. Initially, r(t-1) in CR is set to the full speed, R(1). Thereafter on every clock cycle the comparators QC(1) through QC(n) compare q(t), the quantity of data in buffer B at time t, with the Q(2) through Q(N), respectively, to determine what the current rate code r(t) should be. Suppose that q(t) is greater than Q(2) - Q(4) and less than Q(5) - Q(n). Then the